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(11)

EP 1 014 446 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.06.2000 Bulletin 2000/26

(51) Int Cl.7: **H01L 23/58**(21) Application number: **99310368.8**(22) Date of filing: **21.12.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

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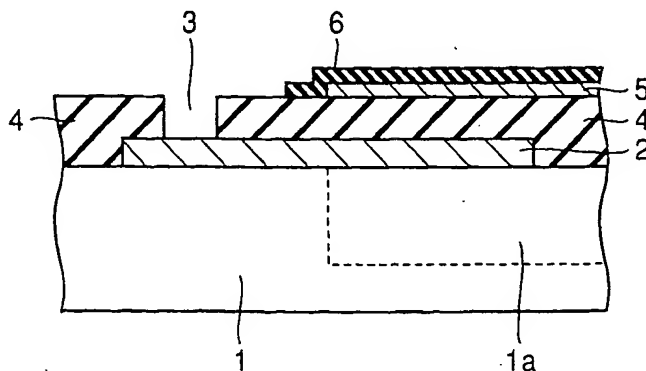
(30) Priority: **21.12.1998 JP 36233598**

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(54) Semiconductor device protected against analysis

(57) A semiconductor device includes a semiconductor substrate (1) having a main circuit part (1a) including a predetermined active element and the like on a silicon substrate, an interconnection (2) transmitting to the active element an externally supplied input signal or transmitting an output signal to be supplied to any external unit, an opening (3) for input/output of the externally supplied signal or the signal to be supplied to any external unit to and from the interconnection (2), an

insulating protection film (4) for protecting the interconnection (2) and an underlying portion thereof, a conductive metal film (5) arranged above the main circuit part (1a), and an aluminum oxide film (6) arranged to cover the conductive metal film (5). This structure can preclude the main circuit part (1a) from being discerned by visual observation, a visible light microscope and an IR microscope, and accordingly imitation, copy and altering of the main circuit part (1a) by other people can be prevented.

FIG. 1**EP 1 014 446 A1**

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to semiconductor devices, and particularly to a semiconductor device configured to prevent analysis of the structure of its circuit component portion and to make it difficult copy or altering of information in the circuit.

Description of the Background Art

[0002] In a semiconductor device, a number of semiconductor elements formed on a substrate with electrode interconnection established are generally protected from influences of ambience such as alpha ray, moisture and stress by covering a circuit component portion with an insulating protection film so as to prevent malfunction due to moisture invasion and the like, change in characteristics caused by stress, and the like. A silicon oxide film, a silicon nitride film and the like are usually employed as the protection film covering the circuit component portion.

[0003] There are some circuit component portions of semiconductor devices which have taken a long period of time for development thereof or which are superior in originality. Therefore, they should preferably be protected from imitation and copy thereof by other people. Further, there is some memory device storing important information in the circuit of the semiconductor device, and thus the information should preferably be protected from being altered.

[0004] However, the insulating protection film mentioned above is provided for protecting the circuit component portion from ambience. Therefore, the film is usually superior in optical transmissivity relative to visible light and far-infrared radiation, so that the circuit component can easily be discerned from above the protection film by a visible light microscope or an IR (infrared) microscope, leading to a high possibility of imitation and copy of the circuit component portion or altering of the information in the memory device.

SUMMARY OF THE INVENTION

[0005] The present invention is made to solve those problems described above. One object of the invention is to provide a semiconductor device having a circuit component portion which is difficult to analyze so as to prevent copy, imitation and altering of information by other people.

[0006] According to one aspect of the present invention, a semiconductor device includes a substrate having a circuit component portion, an insulating protection film formed to cover the circuit component portion, an analysis prevention film formed on the protection film to

cover a main part of the circuit component portion for preventing analysis of the main part, and a corrosion resistant film formed to cover the analysis prevention film for preventing the analysis prevention film from being ruined by a chemical solution.

[0007] Employment of the structure above, which has the analysis prevention film covering the main part, can make it impossible to analyze an underlying circuit pattern.

[0008] According to another aspect of the present invention, a semiconductor device includes a substrate having a circuit component portion, an insulating protection film formed to cover the circuit component portion, and an analysis prevention film formed on the protection film to cover a main part of the circuit component portion for preventing analysis of the main part, the analysis prevention film having corrosion resistance for preventing itself from being ruined by a chemical solution.

[0009] Employment of the above structure can deter an attempt to achieve analysis by performing chemical solution processing on the analysis prevention film for removing the film, since it is difficult to destroy the analysis prevention film by a chemical solution even if a corrosion resistant film is not separately provided.

[0010] Preferably, the semiconductor device according to the invention further includes an interconnection which is placed between the substrate and the protection film to reach the circuit component portion. The protection film has an opening located in a region which is not covered with the analysis prevention film to reach the interconnection. Employment of this structure can deter an attempt to remove the analysis prevention film by the chemical solution processing and thus analyze the circuit pattern, since the chemical solution entering through the opening first removes the interconnection and the circuit component portion.

[0011] Preferably, in the semiconductor device according to the invention, the analysis prevention film and the protection film have their surfaces substantially at the same height. Further, the surface of the protection film is preferably flat. Employment of this structure can prevent an attempt to recognize the entire shape of underlying interconnections and positional relation thereof based on roughness of the surface.

[0012] Preferably, in the semiconductor device according to the present invention, the analysis prevention film is formed of the same material as that of the interconnection. In this structure, if chemical solution processing is performed on the analysis prevention film to eliminate the prevention film, the interconnection could also be eliminated under the same condition and consequently the interconnection disappears before being analyzed. In this way, the analysis can be prevented.

[0013] According to the present invention, preferably the analysis prevention film is formed of an electrically conductive metallic film. Employment of this structure in which the analysis prevention film has a low transmissivity relative to visible light and IR radiation can prevent

analysis of an underlying circuit pattern.

[0014] According to the one aspect of the invention, preferably the electrically conductive metallic film is formed of an electrically conductive metal material. By employing this structure, an analysis prevention film having a low transmissivity relative to visible light and IR radiation can easily be accomplished.

[0015] According to the one aspect of the invention, preferably the electrically conductive metallic film is a metallic film formed of at least one of titanium nitride and titanium-tungsten alloy. Even if the analysis prevention film is not formed of a metal material, employment of the structure above can achieve an analysis prevention film having a low transmissivity relative to visible light and IR radiation.

[0016] According to the one aspect of the invention, the corrosion resistant film is preferably formed of aluminum oxide. Employment of this structure can protect the analysis prevention film from a chemical solution since the aluminum oxide has a superior corrosion resisting effect.

[0017] According to the one aspect of the invention, preferably the corrosion resistant film is formed of dyed aluminum oxide. It is possible to make it further difficult to visibly discern an underlying circuit pattern by employing this structure.

[0018] According to the another aspect of the invention above, preferably the analysis prevention film is formed of an electrically conductive metallic film having corrosion resistance. Further, according to the another aspect of the invention, preferably the electrically conductive metallic film is a metal film formed of at least one of tantalum and niobium. Employment of this structure can accomplish an analysis prevention film having corrosion resistance.

[0019] The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Fig. 1 is a cross sectional view illustrating a main portion of a semiconductor device in a first embodiment of the present invention.

[0021] Figs. 2A to 2I illustrate a process flow of a fabrication procedure in the first embodiment.

[0022] Fig. 3 is a cross sectional view illustrating a main portion of a semiconductor device in Example 1 of a second embodiment of the invention.

[0023] Figs. 4A to 4G illustrate a process flow of a fabrication procedure in Example 1 of the second embodiment.

[0024] Fig. 5 is a cross sectional view illustrating a main portion of a semiconductor device in Example 2 of the second embodiment of the invention.

[0025] Figs. 6A to 6G illustrate a process flow of a fab-

rication procedure in Example 2 of the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] Embodiments of the present invention are now described in detail in conjunction with the drawings.

10 First Embodiment

[0027] Referring to Fig. 1, a semiconductor device in the first embodiment is constituted of a semiconductor substrate 1 having a main circuit part 1a including a predetermined active element and the like on a silicon substrate, an interconnection 2 transmitting to the active element an externally supplied input signal or transmitting an output signal to be supplied to any external unit, an opening 3 for input/output of the externally supplied signal or the signal to be supplied to any external unit to and from interconnection 2, an insulating protection film 4 for protecting interconnection 2 and an underlying portion thereof, a conductive metal film 5 arranged above main circuit part 1a, and an aluminum oxide film 6 arranged to cover conductive metal film 5.

[0028] A fabrication procedure in this embodiment is hereinafter described in conjunction with a process flow shown in Figs. 2A to 2I.

[0029] Referring to Fig. 2A, a conductive metal film such as an aluminum film or the like is deposited to a thickness of 900 nm on semiconductor substrate 1 having the main circuit part by, for example, sputtering. Resist patterning and dry etching are then conducted to form interconnection 2.

[0030] Referring to Fig. 2B, insulating protection film 4 such as a silicon oxide film, a silicon nitride film and the like is deposited to a thickness of 2000 nm on interconnection 2 by, for example, P-CVD (Plasma enhanced CVD).

[0031] Referring to Fig. 2C, the surface of insulating protection film 4 is planed by a thickness of 1000 nm by, for example, CMP (Chemical Mechanical Polishing) to eliminate surface morphology (unevenness of the surface) and accordingly level the surface. It is noted this step is not the indispensable one and thus can be skipped.

[0032] Referring to Fig. 2D, a conductive metal film of the same material as that of interconnection 2, a conductive metal film of another material, or a thin film formed of a material having characteristics similar to those of metal (e.g. titanium nitride film or titanium-tungsten alloy) is deposited to a thickness of 300 nm by, for example, sputtering, and resist patterning and dry etching are conducted to form conductive metal film 5 above the main circuit part.

[0033] Referring to Fig. 2E, the portion where conductive metal film 5 is absent is covered with a patterned resist 7. At this time, the end of the patterned resist 7 is

placed slightly apart from the end of conductive metal film 5 in order to allow conductive metal film 5 to completely be covered with an aluminum oxide film which is formed in the subsequent process step.

[0034] Referring to Fig. 2F, an aluminum film 6' is deposited to a thickness of 150 nm on the entire surface of the substrate by, for example, sputtering.

[0035] Referring to Fig. 2G, aluminum film 6' is oxidized by anodic oxidation. The substrate is immersed in an electrolysis solution of ammonium tartrate or the like, positive voltage of approximately several ten volts is applied to the aluminum film portion on the substrate and thus the portion corresponding to the thickness of the aluminum film is oxidized. Since the oxide film has fine holes, the film is immersed in boiling pure water for hole-fill treatment. In this state, aluminum oxide film 6 is present on the entire surface of the substrate. With this state maintained, aluminum oxide film 6 may be dyed by dye stuff.

[0036] Referring to Fig. 2H, the substrate surface is scrubbed to rub off the oxide film on the resist from the portion at the bottom of the resist with a relatively weak oxide film, and thereafter the resist is removed by using a stripper liquid. If the produced aluminum oxide film pattern has any burr, the substrate surface is scrubbed in this state to remove the burr (lift off method). Cleaning is then carried out to form aluminum oxide film 6 on conductive metal film 5.

[0037] Referring to Fig. 2I, resist patterning and etching of insulating protection film 4 are conducted to form opening 3 for signal input/output.

[0038] In the semiconductor device according to this embodiment, the conductive metallic film formed on the insulating protection film makes it impossible to discern the underlying main circuit part by visual observation, a visible light microscope, and an IR microscope. Further, the aluminum oxide film on the conductive metallic film makes it difficult to remove the metallic film by chemical solution processing. If the chemical solution processing is attempted, the chemical solution first enters through the opening on the underlying interconnection, possibly leading to disappearance of the interconnection itself. In this way, imitation and copy of the main circuit part can be prevented and information in a memory device can be secured (altering of the information can be prevented).

[0039] Further, discerning of the shape of the underlying interconnection can be made impossible by leveling the surface of the insulating protection film.

Second Embodiment

Example 1

[0040] Referring to Fig. 3, a semiconductor device in Example 1 is constituted of a semiconductor substrate 1 having a main circuit part 1a including a predetermined active element and the like on a silicon substrate, an

interconnection 2 transmitting to the active element an externally supplied input signal or transmitting an output signal to be supplied to any external unit, an opening 3 for allowing input/output of the externally supplied signal or the signal supplied to any external unit to and from interconnection 2, an insulating protection film 4 for protecting interconnection 2 and an underlying portion thereof, and a corrosion resistant conductive metal film 8 arranged above main circuit part 1a.

[0041] A fabrication procedure in Example 1 is hereinafter described in conjunction with a process flow shown in Figs. 4A to 4G.

[0042] Referring to Fig. 4A, a conductive metal film such as an aluminum film or the like is deposited to a thickness of 900 nm on semiconductor substrate 1 having the main circuit part by, for example, sputtering. Resist patterning and dry etching are then conducted to form interconnection 2.

[0043] Referring to Fig. 4B, insulating protection film 4 such as a silicon oxide film, a silicon nitride film and the like is deposited to a thickness of 2000 nm on interconnection 2 by, for example, P-CVD.

[0044] Referring to Fig. 4C, the surface of insulating protection film 4 is planed by a thickness of 1000 nm by, for example, CMP to eliminate surface morphology (unevenness of the surface) and accordingly level the surface.

[0045] Referring to Fig. 4D, a depression 4a is formed above the main circuit part by resist patterning and dry etching. A patterned resist 7 is provided as shown. The depth of depression 4a is enough if it is equal to the thickness of a corrosion resistant conductive metal film to be deposited on insulating protection film 4.

[0046] Referring to Fig. 4E, resist 7 is removed, cleaning is conducted, and thereafter corrosion resistant conductive metal film 8, for example, a tantalum film or a niobium film is deposited on the entire surface of the substrate to a thickness of 150 nm.

[0047] Referring to Fig. 4F, the corrosion resistant conductive metal film on the surface of the substrate is planed off by the thickness corresponding to the metal film by metal CMP. By this processing, it is possible to remove only the portion of the corrosion resistant conductive metal film which does not form the depression of the insulating protection film. Consequently, corrosion resistant conductive metal film 8 can be left in the depression only.

[0048] Referring to Fig. 4G, opening 3 for signal input/output is formed by resist patterning and etching of insulating protection film 4.

Example 2

[0049] Referring to Fig. 5, a semiconductor device in Example 2 is constituted of a semiconductor substrate 1 having a main circuit part 1a including a predetermined active element and the like on a silicon substrate, an interconnection 2 transmitting to the active element an

externally supplied input signal or transmitting an output signal to any external unit, an opening 3 for input/output of the externally supplied signal or the signal to be supplied to any external unit to and from interconnection 2, an insulating protection film 4 for protecting interconnection 2 and an underlying portion thereof, and a corrosion resistant conductive metal film 8 arranged above main circuit part 1a. A difference between Example 1 and Example 2 is that no depression is formed in insulating protection film 4 and corrosion resistant conductive metal film 8 is formed on the leveled insulating protection film in the latter.

[0050] A fabrication procedure in Example 2 is now described in conjunction with a process flow shown in Figs. 6A to 6G.

[0051] Referring to Fig. 6A, a conductive metal film such as an aluminum film or the like is deposited to a thickness of 900 nm on semiconductor substrate 1 having the main circuit part by, for example, sputtering. Resist patterning and dry etching are then conducted to form interconnection 2.

[0052] Referring to Fig. 6B, insulating protection film 4 such as a silicon oxide film, a silicon nitride film and the like is deposited to a thickness of 2000 nm on interconnection 2 by, for example, P-CVD.

[0053] Referring to Fig. 6C, the surface of insulating protection film 4 is planed by a thickness of 1000 nm by, for example, CMP to eliminate surface morphology (unevenness of the surface) and thus level the surface.

[0054] Referring to Fig. 6D, corrosion resistant conductive metal film 8, for example, a tantalum film or a niobium film is deposited on the entire surface of the substrate to a thickness of 150 nm by sputtering.

[0055] Referring to Figs. 6E and 6F, resist patterning and dry etching of the corrosion resistant conductive metal film are performed to form corrosion resistant conductive metal film 8 above the main circuit part. Dry etching is effected using CF_4 -based gas.

[0056] Referring to Fig. 6G, resist patterning and etching of insulating protection film 4 are finally conducted to form opening 3 on the interconnection for input/output of signals.

[0057] According to this embodiment, the corrosion resistant conductive metallic film on the insulating protection film prevents the underlying main circuit part from being recognized by visual observation, a visible light microscope and an IR microscope. Further, it is difficult to remove the insulating protection film through chemical solution processing. Even if an attempt to do the chemical solution processing is carried out, the chemical solution first enters through the opening on the underlying interconnection and possibly the interconnection itself disappears. In this way, prevention of imitation and copy of the main circuit part as well as securing of information in a memory device (prevention of altering of the information) are possible. In other words, the second embodiment achieves similar effects to those of the first embodiment even if the aluminum oxide

film is not provided.

[0058] The leveled surface of the insulating protection film can also prevent discerning of the entire shape and positional relation of underlying interconnections.

[0059] Similar techniques are disclosed in Japanese Patent Laying-Open Nos. 9-5770 and 1-214126 and the like. These techniques disclosed are devised in order to protect a semiconductor element from ambience and thus stabilize element characteristics. The element is specifically protected by only a metal film on an insulating protection film and thus those techniques are different from the present invention. Japanese Patent Laying-Open No. 1-165129 discloses a technique devised in order to prevent copy of the circuit component portion similarly to the present invention. However, the structure disclosed is different from that of the present invention. In the former, a protection film formed of the same material as that of an underlying insulating protection film is located on a metal film. Etching of the insulating protection film is stopped when the metal film is exposed, and accordingly etching of only the metal film becomes possible to enable an underlying circuit structure to be discerned.

[0060] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A semiconductor device comprising:

a substrate (1) having a circuit component portion;
an insulating protection film (4) formed to cover said circuit component portion;
an analysis prevention film (5) formed on said protection film (4) to cover a main part (1a) of said circuit component portion for preventing analysis of said main part (1a); and
a corrosion resistant film (6) formed to cover said analysis prevention film (5) for preventing said analysis prevention film (5) from being ruined by a chemical solution.

2. The semiconductor device according to claim 1, further comprising an interconnection (2) located between said substrate (1) and said protection film (4) to reach said circuit component portion, wherein said protection film (4) has an opening (3) located in a region which is not covered with said analysis prevention film (5) to reach said interconnection (2).

3. The semiconductor device according to claim 1,

wherein

said analysis prevention film (5) and said protection film (4) have their surfaces substantially at the same height.

4. The semiconductor device according to claim 1,
wherein said protection film (4) has a flat surface.
5. The semiconductor device according to claim 2,
wherein
said analysis prevention film (5) and said interconnection (2) are formed of the same material.
6. The semiconductor device according to claim 1,
wherein
said analysis prevention film (5) is formed of
an electrically conductive metallic film.
7. The semiconductor device according to claim 6,
wherein
said electrically conductive metallic film is
formed of a conductive metal material.
8. The semiconductor device according to claim 6,
wherein
said electrically conductive metallic film is a
metallic film formed of at least one of titanium nitride
and titanium-tungsten alloy.
9. The semiconductor device according to claim 1,
wherein
said corrosion resistant film is formed of alu-
minum oxide.
10. The semiconductor device according to claim 1,
wherein
said corrosion resistant film is formed of dyed
aluminum oxide.
11. A semiconductor device comprising:

a substrate having a circuit component portion;
an insulating protection film (4) formed to cover
said circuit component portion; and
an analysis prevention film (5) formed on said
protection film (4) to cover a main part (1a) of
said circuit component portion for preventing
analysis of said main part (1a),
said analysis prevention film (5) having corro-
sion resistance for preventing itself from being
ruined by a chemical solution.
12. The semiconductor device according to claim 11,
further comprising an interconnection (2) located
between said substrate (1) and said protection film
(4) to reach said circuit component portion, wherein
said protection film (4) has an opening (3) lo-
cated in a region which is not covered with said

analysis prevention film (5) to reach said intercon-
nection (2).

13. The semiconductor device according to claim 11,
wherein
said analysis prevention film (5) and said pro-
tection film (4) have their surfaces substantially at
the same height.
14. The semiconductor device according to claim 11,
wherein
said protection film (4) has a flat surface.
15. The semiconductor device according to claim 11,
wherein
said analysis prevention film (5) is formed of
an electrically conductive metallic film having cor-
rosion resistance.
16. The semiconductor device according to claim 15,
wherein
said electrically conductive metallic film is a
metal film formed of at least one of tantalum and
niobium.

FIG.1

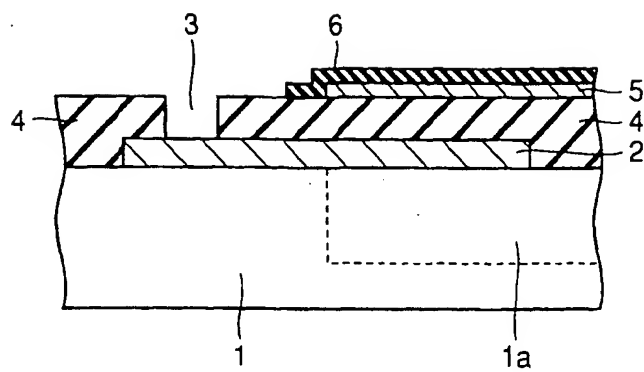


FIG.2A

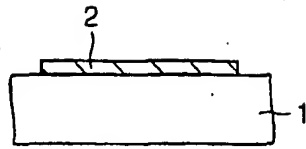


FIG.2B

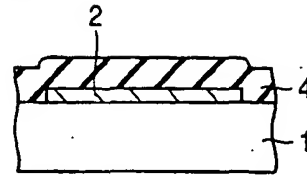


FIG.2C

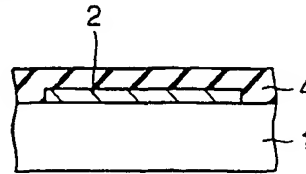


FIG.2D

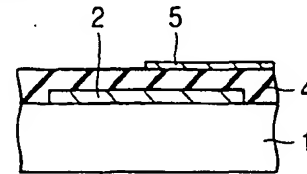


FIG.2E

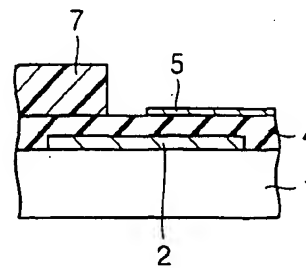


FIG.2F

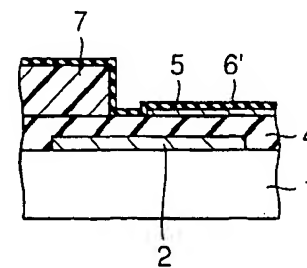


FIG.2G

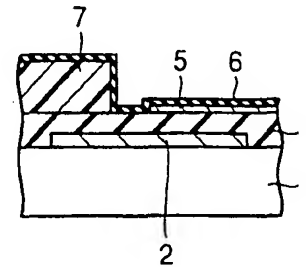


FIG.2H

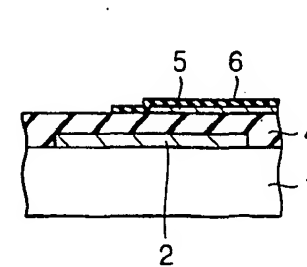


FIG.2I

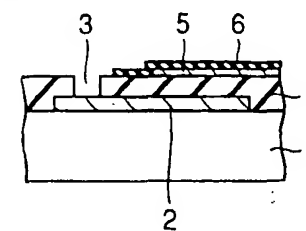


FIG.3

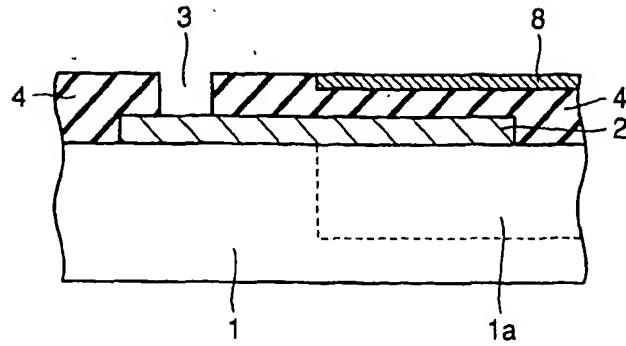


FIG.4A

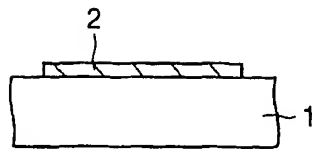


FIG.4B

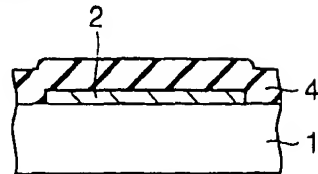


FIG.4C

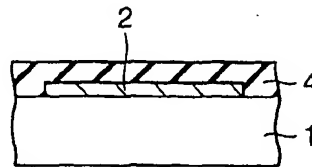


FIG.4D

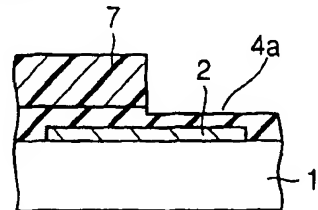


FIG.4E

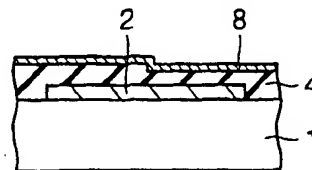


FIG.4F

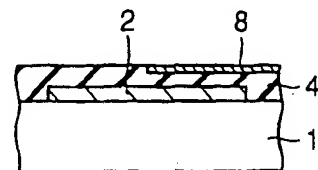


FIG.4G

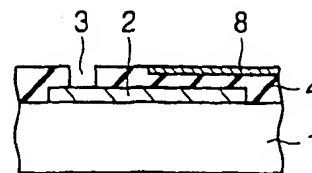


FIG.5

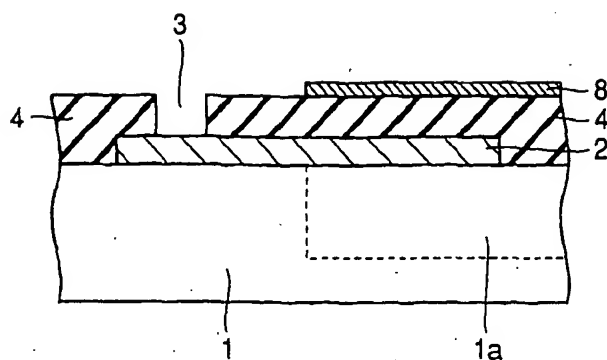


FIG.6A

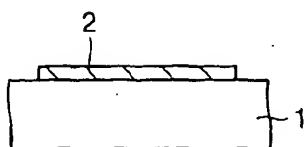


FIG.6B

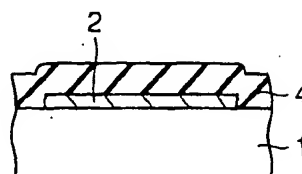


FIG.6C

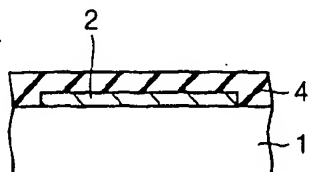


FIG.6D

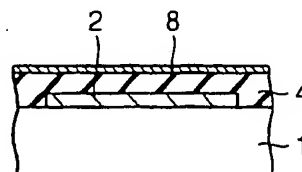


FIG.6E

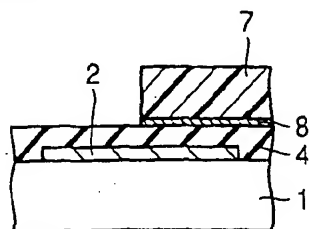


FIG.6F

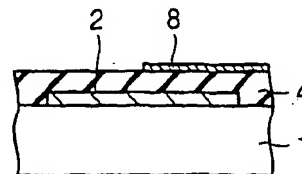
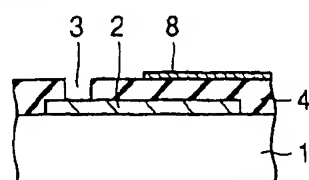


FIG.6G





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 31 0368

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 369 299 A (BYRNE ROBERT C) 29 November 1994 (1994-11-29)	1,2	H01L23/58
A	* column 3, line 3 - column 4, line 52; figure 1 *	6-8,11, 12,15	
D,A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 437 (E-826), 29 September 1989 (1989-09-29) & JP 01 165129 A (SHARP CORP), 29 June 1989 (1989-06-29) * abstract *	1,5	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			H01L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 3 March 2000	Examiner De Raeve, R
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons</p> <p>& : member of the same patent family, corresponding document</p>			

EPO FORM 1503 03/82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 99 31 0368

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

03-03-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5369299 A	29-11-1994	EP 0710401 A WO 9503627 A	08-05-1996 02-02-1995
JP 01165129 A	29-06-1989	NONE	

DOCKET NO: P2001,0087
 SERIAL NO: _____
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